

WHAT IS CLAIMED IS:

1. A memory system, comprising:

- a) at least two ferroelectric memory devices arranged sequentially, wherein:
 - i) each memory device has a data in control signal and a data out control signal;
 - 5 ii) the data out control signal of each memory device is transmitted as the data in control signal of the next device in sequence, terminating with the last device;
- b) a system controller operable to generate an initial data in control signal for the first memory device;
- c) a data bus operable to transfer data between each memory device and the system
10 controller; and
- d) an address bus operable to provide addressing of the memory devices.